CLAIMS

What is claimed is:

1. A content addressable memory (CAM) architecture comprising:

a CAM array including a plurality of rows of CAM cells each coupled to a corresponding match signal line;

a timed storage circuit having data inputs coupled to the match signal lines;

a match comparison timing circuit including a first compare circuit and having an output to assert a first signal indicative of when comparand data matches data stored in at least one of the rows of CAM cells;

a mis-match comparison timing circuit including a second compare circuit and having an output to assert a second signal indicative of when the comparand data mis-matches data stored in at least another one of the rows of CAM cells; and

a select circuit having inputs coupled to receive the first and second signals and an output coupled to the timed storage circuit.

2. The CAM architecture of claim 1, wherein the match comparison timing circuit comprises a plurality of CAM cells that include the first compare circuit.

3. The CAM architecture of claim 1, wherein the mis-match comparison timing circuit comprises a plurality of CAM cells that include the second compare circuit.

4. The CAM architecture of claim 1, wherein the match comparison timing circuit comprises:

a first comparand select circuit for alternatively outputting to the first compare circuit a first comparand and a second comparand;

a first storage circuit for storing first data for comparison with the first and second comparands; and

a first sense circuit coupled to an output of the first compare circuit to sense first compare results between the first data and the first and second comparands.

5. The CAM architecture of claim 4, wherein the mis-match comparison timing circuit comprises:

a second comparand select circuit for alternatively outputting to the second compare circuit a third comparand and a fourth comparand;

a second storage circuit for storing second data for comparison with the third and fourth comparands; and

a second sense circuit coupled to an output of the second compare circuit to sense second compare results between the second data and the third and fourth comparands.

6. A content addressable memory (CAM) architecture comprising:

a CAM array including a plurality of rows of CAM cells each coupled to a corresponding match signal line;

a timed storage circuit having data inputs coupled to the match signal lines;

a first plurality of timing circuits each including a compare circuit and having an output to assert a signal indicative of when comparand data matches data stored in at least one of the rows of CAM cells, wherein each of the first plurality of timing circuit asserts its signal in a different cycle of a clock signal; and

a first interleaver circuit coupled to receive the asserted signals from the first plurality of timing circuits.

7. The CAM architecture of claim 6, wherein each of the first plurality of timing circuits are operable to determine a worst-case period of time of when the comparand data matches data stored in the at least one of the rows of CAM cells.

8. The CAM architecture of claim 6, wherein each of the first plurality of timing circuits are operable to determine a worst-case period of time of when the comparand data mis-matches data stored in the at least one of the rows of CAM cells.

9. The CAM architecture of claim 6, further comprising:

a second plurality of timing circuits each including a compare circuit and having an output to assert a signal indicative of when the comparand data matches data stored in another at least one of the rows of CAM cells, wherein each of the second plurality of timing circuit asserts its signal in a different cycle of the clock signal; and

a second interleaver circuit coupled to receive the asserted signals from the second plurality of timing circuits.

10. The CAM architecture of claim 9, wherein each of the second plurality of timing circuits are operable to determine a worst-case period of time of when the comparand data matches data stored in the at least one of the rows of CAM cells.

11. The CAM architecture of claim 9, wherein each of the second plurality of timing circuits are operable to determine a worst-case period of time of when the comparand data mis-matches data stored in the at least one of the rows of CAM cells.

12. A method, comprising:

forcing a first match signal line coupled to first plurality of content addressable memory (CAM) cells into a match state over a first period of time;

forcing a second match signal line coupled to a second plurality of CAM cells into a mis-match state over a second period of time; and

capturing, after a longer of the first and second periods of time, comparison results on a plurality of match signal lines each coupled to a corresponding row of CAM cells in a CAM array.

13. The method of claim 12, further comprising forcing the first match signal line into a mis-match state before forcing the first match signal line into the match state.

14. The method of claim 12, further comprising forcing the second match signal line into a match state before forcing the second match signal line into the mis-match state.

15. A method, comprising:

forcing a first match signal line coupled to first plurality of content addressable memory (CAM) cells into a mis-match state over a first period of time;

subsequently forcing the first match signal line into a match state over a second period of time; and

capturing, after the second period of time, comparison results on a plurality of match signal lines each coupled to a corresponding row of CAM cells in a CAM array.

16. The method of claim 15, wherein the first period of time spans a plurality of clock cycles.

17. The method of claim 15, wherein the first period of time occurs in a single clock cycles.

18. A method, comprising:

forcing a first match signal line coupled to first plurality of content addressable memory (CAM) cells into a match state over a first period of time;

subsequently forcing the first match signal line into a mis-match state over a second period of time; and

capturing, after the second period of time, comparison results on a plurality of match signal lines each coupled to a corresponding row of CAM cells in a CAM array.

19. A method performed on a content addressable memory (CAM) integrated circuit, comprising:

modeling on the CAM integrated circuit a first worst-case period of time for a row of CAM cells to determine that it stores data that matches first comparand data;

modeling on the CAM integrated circuit a second worst-case period of time for the row of CAM cells to determine that it does not store data that matches the first comparand data; and

capturing, after a longer of the first and second worst-case periods of time, comparison results a match signal line coupled to the row of CAM cells.